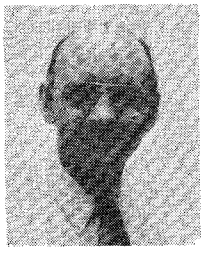

M.S. degree in electrical engineering, the M.S. degree in physics, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 1969 and 1977, respectively.

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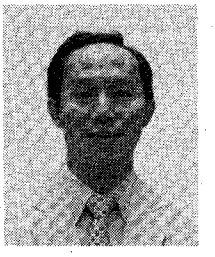

Ph.D. degree in electrical engineering from the University of Michigan, in 1974.

From 1969 to 1973, he was a Research Assistant at the Electron Physics Laboratory, Department of Electrical and Computer Engineering, University of Michigan, Ann Arbor, where he worked on research programs on nonlinear operating characteristics, bias modulation, and self-mixing properties of IMPATT diode oscillators. From 1974 to 1978, he was with the Torrance Research Center, Hughes Aircraft Company, where he worked on millimeter-wave low-noise scanning receivers, high-power pulsed IMPATT sources, and dielectric image-guide integrated circuits. He joined Honeywell Inc., in 1978. He is the Head of GaAs Analog Electronics Section in the Honeywell Corporate Technology Center. He is responsible for the development of microwave and millimeter-wave monolithic integrated circuit technology.

12-GHz-Band Low-Noise GaAs Monolithic Amplifiers

TADAHIKO SUGIURA, HITOSHI ITOH, TSUTOMU TSUJI, AND KAZUHIKO HONJO, MEMBER IEEE

Abstract — **One- and two-stage 12-GHz-band low-noise GaAs monolithic amplifiers have been developed for use in direct broadcasting satellite (DBS) receivers. The one-stage amplifier provides a less than 2.5-dB noise figure with more than 9.5-dB associated gain in the 11.7–12.7-GHz band. In the same frequency band, the two-stage amplifier has a less than 2.8-dB noise figure with more than 16-dB associated gain. A 0.5-μm gate closely spaced electrode FET with an ion-implanted active layer is employed in the amplifier in order to achieve a low-noise figure without reducing reproducibility. The chip size is 1 mm × 0.9 mm for the one-stage amplifier, and 1.5 mm × 0.9 mm for the two-stage amplifier.**

I. Introduction

RECENT ADVANCES in GaAs technology have made monolithic microwave integrated circuits (MMIC's) more practical. Promising applications for this technology include inexpensive receiver front ends for direct broadcasting satellite (DBS) systems [1], [2]. This paper describes design considerations, the fabrication process, and performances for newly developed one- and two-stage 12-GHz-band low-noise GaAs monolithic amplifiers for use in DBS receivers. For MMIC's used in DBS receivers, reproducibility improvement and chip size reduction are essential in order to achieve low cost. A low noise figure is also required for the amplifiers, because it determines the overall receiver noise figure. In this work, most efforts were focused on achieving these requirements.

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II. FET Design

The main reason for poor MMIC reproducibility is the variation in FET characteristics caused by nonuniformity of active layers. To improve uniformity, an ion-implantation technique was employed to form the active layers, although epitaxially grown active layers are believed to be better for low-noise FET's. In conventional MMIC's, a recessed gate structure has been widely used for reducing unfavorable source resistance [5]. The gate-recessing process, however, degrades uniformity of active layers. To overcome this difficulty, a closely spaced electrode (CSE) FET structure [3], [4] was introduced. In the CSE FET, source–gate and drain–gate spacings are shortened to 0.5

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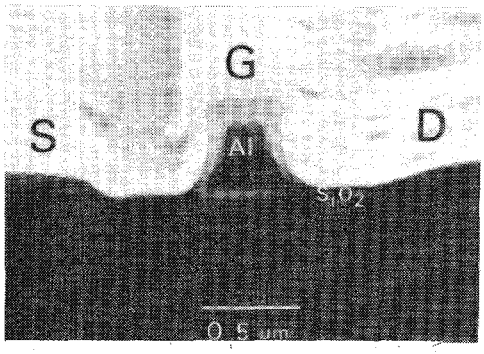

Fig. 1. CSE FET cross-sectional SEM photograph.

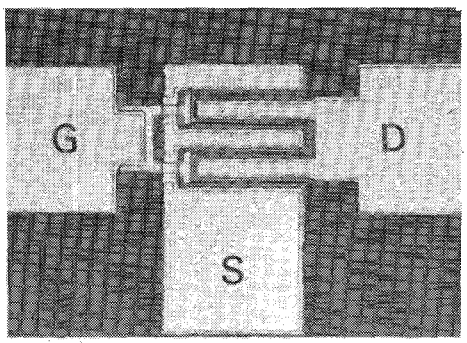

Fig. 2. FET electrode pattern.

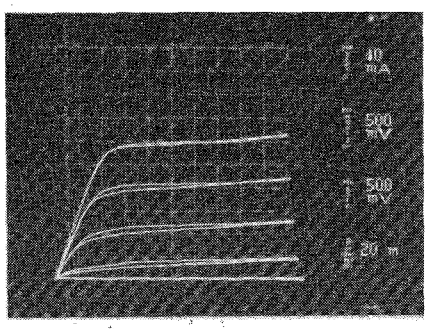

Fig. 3. FET static characteristics.

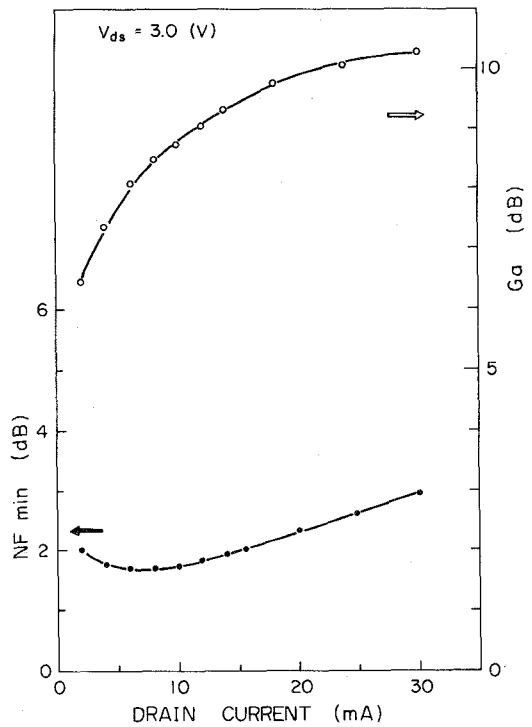

Fig. 4. FET minimum noise-figure and associated gain characteristics.

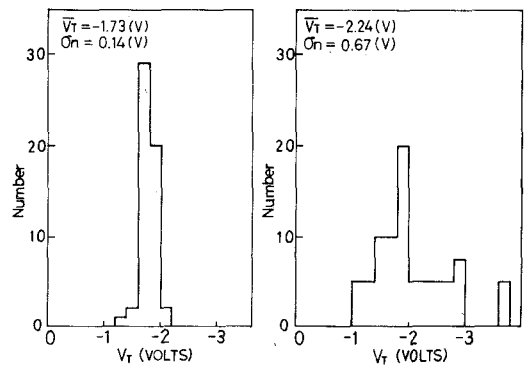

Fig. 5. Histograms showing threshold voltage distributions for CSE FET and deeply recessed epi-FET. (a) Ion-implanted wafer. (b) Epitaxial wafer.

μm, so that source resistance can be reduced sufficiently without recessing the gate. Fig. 1 is a cross-sectional SEM photograph of the FET. The gate was formed 0.5 μm long by side-etching from a 1.5-μm-long photoresist mask. The mask was also utilized to form ohmic electrodes. Because the ohmic electrodes are formed by lifting-off technique, source–drain spacing becomes 1.5 μm long and the gate is formed at the center of the spacing. Therefore, the gate and the ohmic electrodes were self-aligned.

Although a bar-shaped gate pattern is usually used in discrete low-noise FET's [5], an interdigital electrode pattern has been employed because this pattern uses less space. As shown in Fig. 2, the FET has four gate fingers. Each finger is 70 μm long. The total gate width is 280 μm. An FET threshold voltage V_t has been chosen as -1.7 V. Fig. 3 shows static characteristics for the FET. The saturated drain current I_{dss} is 60 mA. Observed transconductance g_m at a 10-mA drain current is 30 mS, which corresponds to 105 mS/mm. Gate breakdown voltage V_{bg} is -8.5 V. Source resistance R_s and source-to-gate capacitance C_{sg} at 0-V bias voltage are 4 Ω and 0.23 pF, respectively. Microwave characteristics were measured at 12 GHz. Results are shown in Fig. 4. The minimum noise figure $NF_{\min}$ and associated gain Ga at a 10-mA drain current are 1.7 and 8.8 dB, respectively. Maximum available gain (MAG) at a 30-mA drain current is 11.5 dB. These characteristics are almost the same as for the deeply recessed epi-FET [5].

In order to study orientation effects [6], FET's oriented in both [011] and [01$\bar{1}$], crystal directions were fabricated and measured. However, both for static and microwave characteristics, no significant difference was observed.

In Fig. 5, histograms showing V_t distributions on a wafer for the CSE FET and the deeply recessed epi-FET are comparatively presented. Averaged threshold voltage $\bar{V}_t$

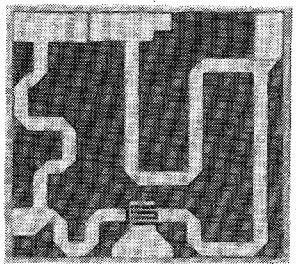

Fig. 6. One-stage amplifier chip photograph.

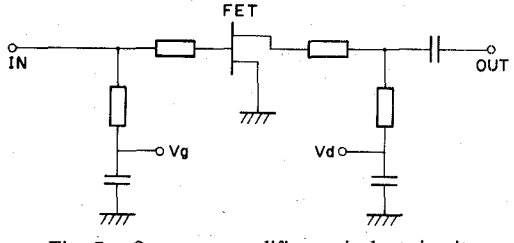

Fig. 7. One-stage amplifier equivalent circuit.

and standard deviation σ_n for the CSE FET are -1.73 and 0.14 V, respectively. For the epi-FET, they are -2.24 and 0.67 V, respectively. A sample variation coefficient defined by $\sigma_n/\bar{V}_t$, which is a measure for achieving uniformity, is 0.08 for the CSE FET and 0.30 for the epi-FET. Therefore, the uniformity in the CSE FET is improved by a factor of approximately four compared with the epi-FET.

When ion-implanting conditions are fixed, reproducibility in FET threshold voltages for two wafers sliced from different ingots is rather poor, because physical parameters, especially Cr concentration, for each ingot are greatly different. Also, in one ingot, the Cr concentration at the top and bottom positions are considerably different, because it varies along the crystal growth direction. Therefore, the implanting conditions have been experimentally determined by test implantation into several wafers sampled from an ingot. By this procedure, the desired FET threshold voltage can be realized with good reproducibility for all the remaining wafers in the ingot.

III. Amplifier Design

Fig. 6 shows a chip photograph for the one-stage amplifier. Fig. 7 shows its equivalent circuit. The chip size is 1 mm $\times$ 0.9 mm, and the wafer thickness is 150 μm. One-section parallel and series microstrip lines are used for matching circuits. These lines can also be utilized as dc-bias feed lines. This arrangement allows a great savings in the chip area. To retain a high Q value, a 2.5-μm metallization thickness was chosen. The measured Q value for a 50-μm-wide line, which was mostly used in the amplifier, is 30 ~ 40 at 12 GHz. This value is somewhat lower than the value estimated from data described in [7]. As shown, the microstrip lines were folded in order to reduce the chip size. To avoid parasitic couplings, the spacings between adjacent lines were designed to be as large as possible.

Capacitors are of the MIM type, where dielectric material is SiO_2, with a relative dielectric coefficient ϵ_r of 4.8.

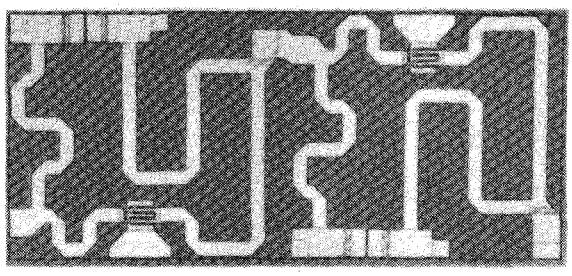

Fig. 8. Cascaded version of the two-stage amplifier chip photograph.

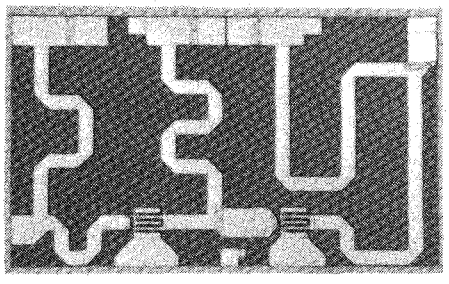

Fig. 9. Modified version of the two-stage amplifier chip photograph.

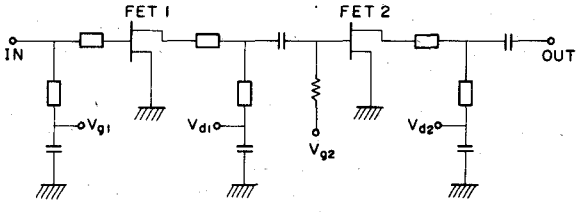

Fig. 10. Modified version of the two-stage amplifier equivalent circuit.

Measured Q values for a 1.42-pF capacitor are 31.3 at 2.5 GHz, 28.8 at 5.4 GHz, and 27.1 at 8.6 GHz. For a 4.2-pF capacitor, they are 22.6 at 2.1 GHz, 17.2 at 5.2 GHz, and 17.0 at 8.4 GHz. The measurement was carried out by employing a resonant method [8]. All capacitors are used as dc-block or RF-short capacitors. Therefore, capacitance has been chosen larger than 2 pF and thickness control for SiO_2 film is not critical.

By using measured S-parameters for a discrete FET, element values in a FET equivalent circuit were derived. Based on these values, the amplifier circuit parameters were optimized by a CAD program. In the desired frequency band, which is from 11.7 to 12.7 GHz, more than a 9-dB gain was predicted.

There are two different versions of the two-stage amplifier. One is constructed through a cascaded connection between two identical one-stage amplifiers, as shown in Fig. 8. Therefore, the chip is double sized at 2 mm $\times$ 0.9 mm. In this version, the impedance locus from the first- to second-stage FET passes through a 50-Ω point. This route is obviously redundant. Therefore, chip size reduction can be expected by modifying the interstage matching circuit, as the route becomes shorter. In the other version, the modification was carried out by using the CAD program. A chip photograph and its equivalent circuit for the modified version are shown in Fig. 9 and Fig. 10, respectively. As shown, the chip size is reduced to 1.5 mm $\times$ 0.9 mm,

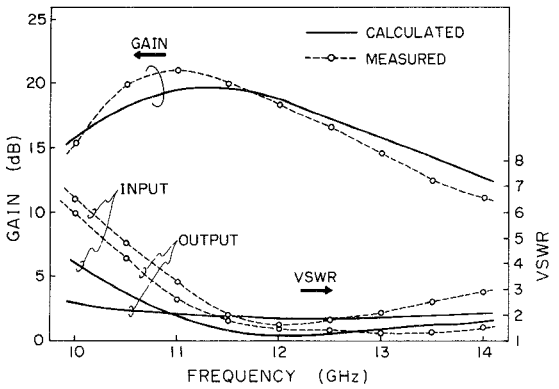

Fig. 11. Comparison between calculated and measured characteristics in modified version of the two-stage amplifier.

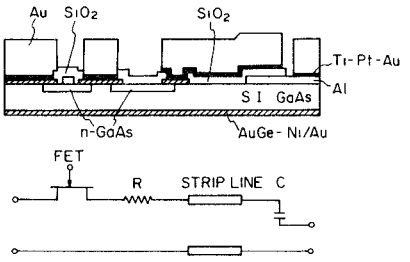

Fig. 12 Circuit elements cross-sectional view and equivalent circuit.

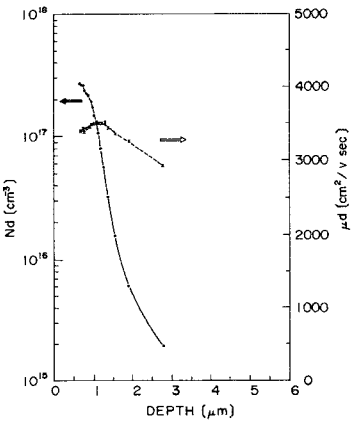

Fig. 13. Carrier concentration and drift mobility profiles

although the matching element sensitivity becomes slightly higher. Gate-bias voltage for the second-stage FET is supplied through a resistor. The resistance was chosen larger than 5 kΩ to prevent causing dissipation loss.

Fig. 11 shows a comparison between calculated and measured characteristics for gain and VSWR's in the modified version two-stage amplifier. As shown, quantitative designability is poor, although qualitative tendencies agree well. The poor designability is caused by inaccuracy in FET S-parameter measurement and by parasitic couplings between matching elements. Therefore, in actual design, the matching circuit pattern layout, including noise-matched operation, has been determined by experimental modification from original gain-matched CAD data. This layout modification can be accomplished by changing only one photomask level at the final fabrication process. Usually, desired characteristics are obtained after one to two modifications.

IV. Fabrication Process

Fig. 12 shows a cross-sectional view for various circuit elements together with their equivalent circuit. A Cr-doped semi-insulating HB-grown GaAs wafer is selectively implanted with $^{30}Si^{+}$ to form FET active layers. Resistive layers are formed at the same time. Implanting conditions for realizing $V_T = -1.7$ V are a 70-keV acceleration energy and a 3.2×10^{12} cm^{-2} dose. The wafer is then annealed with a 0.2-μm-thick CVD-SiO_2 cap at 800° C for 20 min in a H_2 ambient. Donor carrier concentration N_d and drift mobility μ_d profiles in the ion-implanted layer are shown in Fig. 13. They were measured by using a 250-μm-long gate FET [9]. The peak carrier concentration is 2.7×10^{17} cm^{-3} and the mobility is about 3500 cm^2/V·s.

Al, which is used as FET gates and capacitor lower electrodes, is deposited by vacuum evaporation to 0.4-μm thickness and etched to form the gates. Ohmic electrodes for the FET's and the resistors are then formed by lifting off a AuGe-Ni film and alloying it at 400° C. In GaAs IC fabrication, the gate-forming process is usually most difficult. In this process, however, it is very simple because the gates and the ohmic electrodes are self-aligned, as previously mentioned. After ohmic electrodes are formed, the Al is gain etched to form the capacitors lower electrodes. Then, SiO_2 for FET passivation and capacitor dielectric material is chemically vapor-deposited to a 0.2-μm thickness and etched to form contact vias. Next, Ti for the electroplating feeder is evaporated onto the whole wafer. Microstrip lines and capacitor upper electrodes are then formed by Ti-Pt-Au liftoff and thickened to 2.5 μm by selective Au plating. Topside processing is completed by etching off the feed metal Ti. The wafer is thinned and the rear is metallized by AuGe–Ni–Au evaporation. Amplifier chips can be obtained by cleaving the wafer.

V. Microwave Performance

Amplifier chips were chosen for microwave evaluation on the basis of visual inspection and dc testing. The selected chips were mounted on Au-plated copper carriers using AuSn solder. The carriers were then mounted on test fixtures and tested in a 50-Ω system. Needless to say, no external bias tee is necessary, because bias circuits are included on the chips.

Fig. 14 shows gain and noise figure characteristics for the one-stage amplifier. In the 11.7–12.7-GHz band, which is the desired frequency band, the amplifier provides a less than 2.5-dB noise figure with more than 9.5-dB associated gain. The maximum gain and the minimum noise figure in the band are 12 and 2.2 dB, respectively. Bias conditions are 2.5-V drain voltage and 10-mA drain current. Although the gain can be increased by increasing the drain voltage, as well as the drain current, when this increase is made, the noise figure is degraded. The noise figure was measured at 70-MHz IF frequency using a mixer. Input and output VSWR's are less than 3, and less than 2.5 in the desired frequency band, respectively.

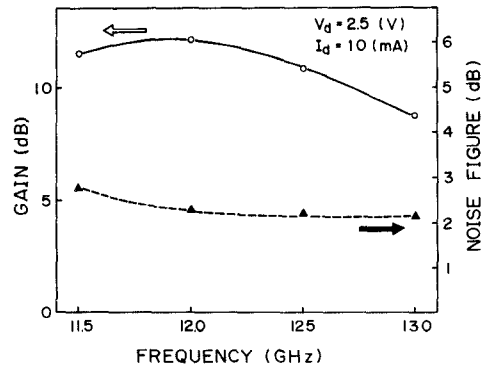

Fig. 14. One-stage amplifier gain and noise-figure characteristics.

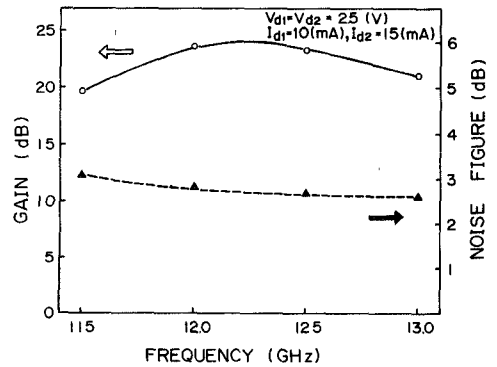

Fig. 15. Cascaded version of the two-stage amplifier gain and noise-figure characteristics.

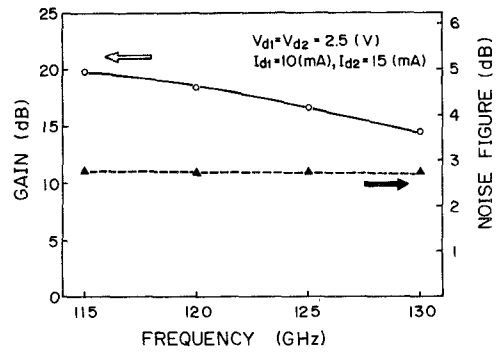

Fig. 16. Modified version of the two-stage amplifier gain and noise-figure characteristics.

Gain and noise figure characteristics for the cascaded version two-stage amplifier are shown in Fig. 15. More than a 20-dB gain with a 24-dB maximum, and less than a 3-dB noise figure with 2.6-dB minimum are obtained in the desired band. The input VSWR is less than 4, and the output VSWR is less than 2.5. These characteristics mostly agree with the value predicted from the one-stage amplifier, because this version is constructed simply by the cascaded connection. For two-stage amplifiers, the drain current for the second-stage FET is set at 15 mA.

Fig. 16 shows gain and noise figure characteristics for the modified version two-stage amplifier. In the desired frequency band, the amplifier has less than a 2.8-dB noise figure with more than a 16-dB associated gain. Although the gain is degraded, compared with the cascaded version, the noise figure is improved. Input and output impedances

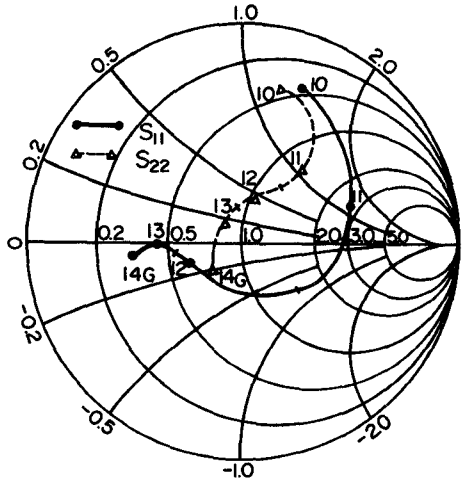

Fig. 17. Modified version of the two-stage amplifier input and output impedances.

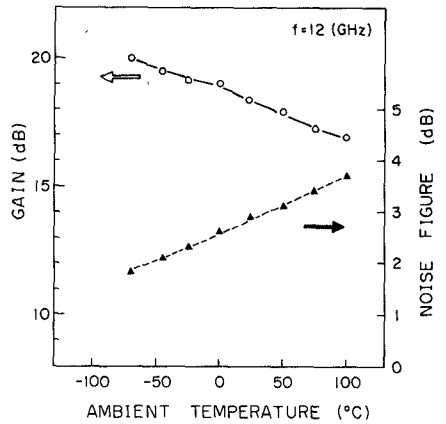

Fig. 18. Modified version of the two-stage amplifier temperature characteristics.

for this amplifier are shown in Fig. 17. In the figure, reference planes are chosen at cleaved edges of the amplifier chip. Less than 2.5 input VSWR and less than 2 output VSWR are obtained in the 11.7–12.7-GHz band.

Fig. 18 shows gain and noise figure versus ambient temperature characteristics at a 12-GHz frequency for the modified version two-stage amplifier. In the measurement, drain currents, which varied with the ambient temperature, were set to standard values at room temperature. At −70° C, the noise figure is 1.8 dB, with a 20-dB associated gain. While at 100° C, the noise figure is 3.7 dB with a 16.9-dB associated gain. Between these temperatures, the gain and noise figure are changed linearly according to changes in ambient temperature. These tendencies are almost the same for frequencies other than 12 GHz. Therefore, frequency characteristics both for the gain and the noise figure are shifted in parallel when varying the ambient temperature.

VI. Conclusion

The design considerations, fabrication process, and performances for newly developed one- and two-stage 12GHz-band low-noise GaAs monolithic amplifiers for use in DBS receivers have been described. By introducing the ion-implanted CSE FET, both a low noise figure and im-

proved uniformity, which implies high reproducibility, can be achieved. Chip size reduction is also accomplished by employing compact matching circuits. The measured microwave performances are well within the acceptable range for DBS receivers. Although the investigation on yields has not been sufficiently carried out, it is believed that this approach has the potential to obtain good results. This work has made a cost-effective one-chip front end for DBS systems more realistic.

ACKNOWLEDGMENT

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REFERENCES

[1] K. Kermarrec, P. Harrop, C. Tsironis, and J. Faguat, "Monolithic circuits for 12 GHz direct broadcasting satellite reception," in *Microwave and Millimeter-Wave Monolithic Circuits Symp., Dig. Papers*, June 1982, pp. 5–10.

[2] L. C. Liu, D. W. Maki, M. Feng, and M. Siracusa, "Single and dual stage monolithic low noise amplifiers," in *GaAs IC Symp. Tech. Dig.*, Nov. 1982, pp. 94–97.

[3] T. Furutsuka, T. Tsuji, F. Katano, A. Higashisaka, and K. Kurumada, "Ion-implanted E/D type GaAs IC technology," *Electron. Lett.*, vol. 17, no. 25/26, pp. 944–945, Dec. 1981.

[4] K. Honjo, T. Sugiura, T. Tsuji, and T. Ozawa, "Low-noise low-power-dissipation GaAs monolithic broadband amplifiers," in *GaAs IC Symp. Tech. Dig.*, Nov. 1982, pp. 87–900.

[5] K. Ohata, H. Itoh, F. Hasegawa, and Y. Fujiki, "Super low-noise GaAs MESFET's with a deep-recess structure," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1029–1034, June 1980.

[6] C. P. Lee, R. Zucca, and B. M. Welch, "Orientation effect on planar GaAs Schottky barrier field effect transistors," *Appl. Phys. Lett.*, vol. 37, no. 3, pp. 311–313, Aug. 1980.

[7] A. Higashisaka and T. Mizuta, "20-GHz band monolithic GaAs FET low-noise amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-29, pp. 1–6, Jan. 1981.

[8] R. E. DeBrecht, "Impedance measurements of microwave lumped elements from 1 to 12 GHz," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-20, pp. 41–48, Jan. 1972.

[9] R. A. Pucel and C. F. Krumm, "Simple method of measuring drift-mobility profiles in thin semiconductor films," *Electron. Lett.*, vol. 12, no. 10, pp. 240–242, May 1976.

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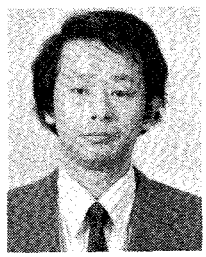

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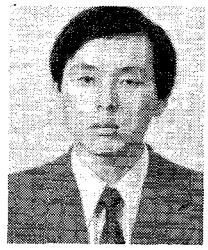

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